AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 5, lines 23-30 as follows:

Referring now to FIG. 3A, an interlayer insulating film ~~11~~ 31 is formed on a substrate 30. A plurality of damascene patterns 32 having different densities are then formed in the interlayer insulating film 31 by means of a damascene scheme. Next, a copper barrier metal layer 33 and a copper seed layer 34 are sequentially formed along the surface of the interlayer insulating film 31 including the plurality of the damascene patterns 32. Thereafter, a copper layer 35 is formed by means of a copper electroplating method so that the plurality of the damascene patterns 32 in which the copper seed layer 34 is formed are sufficiently filled.

Please amend the paragraph at page 6, lines 21-28 as follows:

In the above, the electro-polishing process includes polishing the copper layer 35 using a target thickness in the range of 5000 ~ 15000Å same or similar to the plating thickness in a state that the positive (+) power supply having current in the range of 1 ~ 30A is applied to the wafer. At this ~~tine~~ time, due to application of the positive (+) power supply, the potential is concentrated on the projections along the shape of the surface of the wafer, i.e., the shape of the surface of the copper layer 35. As the rate of the electro-polishing process at the projections becomes thus faster than those at the flat portions, the copper layer 35 is flat over the entire wafer.